Attorney Docket No. : I002.P021U1
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Lucck, David**	
Serial No. **10/697,503**	Group Art Unit: **2185**
Filed: **10/30/2003**	Examiner: **YU, Jae Un**
For: **"Pipeline Recirculation for Data Mispredict ion in a Fast-Load Data Cache"**	Customer Number: **25854**

AMENDMENT AND RESPONSE TO OFFICE ACTION

Commissioner for Patents
Mail Stop Amendment
P.O. Box 1450
Alexandria, VA 22313-1450

April 20, 2006

Sir,

In response to the Official Action dated January 20, 2006, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 6 of this paper.

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0025] with the following amended paragraph:

[0025] Fig. 3 is a block diagram illustrating the fast-load data cache physical layout on a processor core chip area with the fast-load data caches, ~~sown~~ shown here as 1KB LD BUF A 13 and 1KB LD BUF B 15, near the ALUs 26,30 to meet the requirement that the fast-load data caches 13,15 that must access and forward in one cycle just as the ALUs 26,30 do. Special care is taken to select the cache address for the next data cache access so that the most critical address bits to be very close to the AGEN logic to initiate the next cache access (LBUFILO or L1) quickly. Register files 16,18 are also in close proximity to the ALUs 26,30 so that the correct data can be latched without cycle penalty upon a correct speculative guess load.

AMENDMENTS TO THE CLAIMS

Please Cancel Claims 1, 9 and 15-16 without prejudice. Please Add new Claims 17 and 18. Please Amend the claims according to the following listing. This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (Cancelled)

2. (Currently Amended) The system of claim ~~1~~ 17, wherein the speculative data load is loaded in the pipeline ~~one or more pipelines~~.

3. (Currently Amended) The system of claim ~~1~~ 17, wherein one or more of the data loads in the pipeline ~~one or more pipelines~~ are not dependent on any specific data load and not selectively flagged.

4. (Currently Amended) The system of claim ~~1~~ 17, wherein the flag is a bit within the instruction ~~data load~~.

5. (Currently Amended) The system of claim ~~1~~ 17, wherein the flag is attached to the instruction ~~data load~~.

6. (Currently Amended) The system of claim ~~1~~ 17, wherein each flagged instruction ~~the flagged dependent specific data load~~ is flushed from the pipeline ~~one or more pipelines~~ upon the determination of a misprediction for a data load.

7. (Original) The system of claim ~~1~~ 17, wherein the fast-load data cache includes a directory.

8. (Original) The system of claim ~~1~~ 17, wherein the fast-load data cache does not include a directory.

9. (Cancelled)

10. (Currently Amended) The method of claim ~~9~~ 18, further comprising the step of loading the speculative data load into the pipeline.

11. (Currently Amended) The method of claim ~~9~~ 18, wherein the step of selectively flagging the one or more instructions does not flag an instruction that is not dependent on a specific instruction. ~~data loads does not flag any data load that is not dependent on any specific data load~~

12. (Currently Amended) The method of claim ~~9~~ 18, wherein the step of selectively flagging a dependant instruction ~~the data load~~ occurs through altering a bit within the dependant instruction ~~data load~~.

13. (Currently Amended) The method of claim ~~9~~ 18, wherein the step of selectively flagging the dependant instruction ~~data load~~ occurs through attaching a flag to the dependant instruction ~~data load~~.

14. (Currently Amended) The method of claim ~~7~~ 18, further comprising the step of flushing

the flagged dependent instruction ~~specific data load~~ from the pipeline upon the determination of a misprediction of a corresponding data load.

15-16. (Cancelled)

17. A computer architecture, comprising:

at least one pipeline able to selectively load, execute and flush as series of instructions and capable of selectively flagging each of the series of instructions with a flag to indicate dependence upon the load of a speculative instruction;

at least one fast-load data cache that loads at least one speculative data load relative to the speculative instruction;

a circuit that determines if the speculative data load is a misprediction; and

the pipeline being constructed so that if the speculative data load is a misprediction, then execution of the dependant instruction is inhibited while the dependant instruction is in the pipeline, otherwise executing the dependant instruction.

18. A method for executing instructions in a computer architecture that includes a pipeline, the method comprising the steps of:

loading a plurality of instructions into the pipeline;

selectively flagging a dependant instruction in the pipeline, thereby indicating that the dependant instruction depends upon the load of a speculative instruction

loading a speculative data load relative to the speculative instruction;

determining if the speculative data load is a misprediction; and

inhibiting execution of the dependant instruction while the dependant instruction is in the pipeline if the speculative data load is a misprediction, otherwise executing the

dependant instruction.

REMARKS

Claims 2-8, 10-14 and 17-18 remain in the application. Support for the new claims and other amendments may be found, for example, in paragraphs [0033] and [0034], and the corresponding figures. The Specification was amended to correct a typographical error in paragraph [0025]. Applicant asserts that no new matter has been added. Reconsideration of the Application is hereby requested

Objections to the Specification

The Specification was objected to as containing a spelling error in paragraph 25. The Specification has been amended according to the Examiner's suggestion. Therefore, it is believed that this objection has been overcome and Applicant respectfully requests that it be withdrawn.

Claim Rejections

Rejections Under 35 U.S.C. § 112, ¶ 1

Claim 15 was rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Claim 15 has been cancelled without prejudice, thereby rendering this rejection moot.

Rejections Under 35 U.S.C. § 112, ¶ 2

Claims 14-16 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Regarding the rejection as applied to Claim 14, Applicant has amended Claim 14 to depend from new Claim 18. It is believed that this amendment overcomes this rejection and Applicant

respectfully requests that it be withdrawn.

Regarding the rejection as applied to Claim 15 and 16, as these claims have been cancelled, this rejection has been rendered moot with respect to these claims.

Rejections Under 35 U.S.C. § 103

Claims 1-6 and 9-14 were rejected under 35 U.S.C. § 103(a), as being obvious over Peir et al., in view of Au. Applicant has cancelled Claims 1 and 9. New Claims 17 and 18 have been added. Applicant will address the rejection as though it had been applied to Claims 17 and 18.

Peir discloses a system in which a processor can schedule a dependant instruction before a parent instruction executes, speculating that the load will hit the cache. [¶0012] A cache hit/miss prediction table (CPT) is maintained and if a CPT "entry indicates a miss, the dependent instructions are canceled and recovered in the next cycle." [¶0016] The fact that they are recovered in the next cycle indicates that they are cancelled while in the cache and are not yet in the pipeline, otherwise the recovery would take the number of cycles equal to the latency of the pipeline. While Peir mentions that its system may be used in association with a pipeline architecture, Peir does not disclose a system that inhibits execution of mispredicted instructions that have already been fed into the pipeline. An architecture of the type disclosed in Peir would still require a complete pipeline flush if it were determined that a misprediction had occurred relative to an instruction and, thus, Peir would not solve the problem of requiring an entire pipeline to be flushed upon the occurrence of a misprediction.

The present invention, as claimed in new independent Claims 17 and 18, on the other hand, provides for a mechanism in which all instructions in a pipeline (even those that are affected by a misprediction) are allowed to propagate through the pipeline. The valid instructions are allowed to execute, whereas instructions dependant on a mispredicted event are inhibited from executing. This avoids the flushing of an entire pipeline every time that a

misprediction occurs.

Nowhere does Peir or Au teach or suggest, either alone or in combination, the limitation of "the pipeline being constructed so that if the speculative data load is a misprediction, then execution of the dependant instruction is inhibited while the dependant instruction is in the pipeline," as recited in Claim 17, or the limitation of "inhibiting execution of the dependant instruction while the dependant instruction is in the pipeline if the speculative data load is a misprediction, otherwise executing the dependant instruction," as recited in Claim 18. For these reasons, it is believed that this rejection has been overcome and Applicant respectfully requests that it be withdrawn.

Claim 7 was rejected under 35 U.S.C. § 103(a), as being obvious over Peir et al., in view of Au and further in view of "The Cache Memory Book." Because Claim 7 depends from Claim 17, which Applicant believes is now in condition for allowance, Applicant also believes that this rejection has been overcome and respectfully requests that it be withdrawn.

Claim 8 was rejected under 35 U.S.C. § 103(a), as being obvious over Peir et al., in view of Au and further in view of "The Cache Memory Book." Because Claim 8 depends from Claim 17, which Applicant believes is now in condition for allowance, Applicant also believes that this rejection has been overcome and respectfully requests that it be withdrawn.

CONCLUSION

Applicant believes that the rejections have been overcome for the reasons recited above. Therefore, Applicant respectfully requests that all remaining claims be allowed and that a timely Notice of Allowance be issued.

No addition fees are believed due. However, the Commissioner is hereby authorized to charge any additional fees that may be required, including any necessary extensions of time, which are hereby requested, to Deposit Account No. 503535.

04/20/2006
Date

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